CLAIMS

What is claimed is:

1. A method comprising:

determining if a predetermined limit of global functional activity in an integrated circuit has been met or exceeded;

and if so, then

reducing a high frequency of clocking of circuitry gradually to zero to stop the clocking of circuitry,

waiting a predetermined time after stopping the clocking of circuitry, and

starting the clocking of circuitry at a low frequency.

2. The method of claim 1, wherein

if the determining if the predetermined limit of global functional activity in the integrated circuit has not been met or exceeded, it is repeated.

3. The method of claim 1, wherein

the predetermined time is a number of clock cycles of a free-running clock of the integrated circuit.

4. The method of claim 1 wherein,

the reducing of the high frequency clocking of circuitry gradually to zero includes

clocking circuitry at a first frequency, and,

before clocking the circuitry at a second frequency lower than the first frequency,

waiting a predetermined time during the clocking of the circuitry at the first frequency.

5. The method of claim 1, wherein,

after starting the clocking of the circuitry at the low frequency, the method further includes

gradually increasing the frequency of the clocking of the circuitry to the high frequency.

6. The method of claim 5 wherein,

the gradual increasing of the frequency of the clocking of circuitry to the high frequency includes

clocking circuitry at a first frequency, and,

before clocking the circuitry at a second frequency higher than the first frequency,

waiting a predetermined time during the clocking of the circuitry at the first frequency.

7. The method of claim 1, wherein,

global functional activity in the integrated circuit is proportional to temperature of the integrated circuit and

the predetermined limit of global functional activity is proportional to an expected temperature level of the integrated circuit.

8. The method of claim 1, wherein

the reducing of the high frequency clocking of the circuitry gradually to zero avoids large variations in current otherwise associated with a rapid shut-off of the clocking of circuitry.

9. The method of claim 5, wherein

the starting of the clocking of the circuitry at the low frequency and the gradual increase in the frequency of the clocking of the circuitry to the high frequency avoids

large variations in current otherwise associated with a rapid turn-on of the clocking of circuitry.

10. An integrated circuit comprising:

a clock generator to generate a clock;

an activity detector to measure global functional activity of the integrated circuit; and

a clock throttling controller coupled to the activity detector and the clock generator, the clock throttling controller to generate a throttled clock to couple to functional blocks of the integrated circuit for clocking circuitry therein, the clock throttling controller to gradually throttle the frequency of the throttled clock to the functional blocks in response to the measure of the global functional activity meeting or exceeding a predetermined limit.

11. The integrated circuit of claim 10, wherein,

the activity detector receives measures of local functional activity associated with each functional block of the integrated circuit to measure the global functional activity of the integrated circuit.

12. The integrated circuit of claim 10, wherein,

the activity detector receives measures of local functional activity associated with each functional block of the integrated circuit to determine the measure of the global functional activity of the integrated circuit,

the activity detector compares the measure of the global functional activity with the predetermined limit to determine if it is met or exceeded, and

the activity detector signals to the clock throttling controller whether or not the predetermined limit has been met or exceeded.

13. The integrated circuit of claim 10, further comprising,

a logical gate coupled to the clock generator to receive the clock and the clock throttling controller to receive a control signal, the logical gate to periodically mask out one or more clock cycles of the clock to generate the throttled clock in response to the control signal to gradually throttle the frequency of the throttled clock.

14. The integrated circuit of claim 13, wherein,

the logical gate is an AND gate to logically AND the clock and the control signal from the clock throttling controller together.

15. The integrated circuit of claim 10, wherein,

one hundred percent of the circuitry in the functional blocks can have the throttled clock stopped.

16. The integrated circuit of claim 10, wherein,

less than one hundred percent of the circuitry in the functional blocks can have the throttled clock stopped.

17. The integrated circuit of claim 16, wherein,

only the circuitry to which the throttled clock can be stopped is the throttled clock coupled and its frequency gradually throttled in response to the measure of the functional activity meeting or exceeding the predetermined limit.

18. The integrated circuit of claim 10, wherein,

the frequency of the throttled clock is gradually throttled OFF and then ON in response to the measure of the functional activity meeting or exceeding the predetermined limit.

19. A clock generator comprising:

a free-running clock generator to generate a free-running clock;

a thermal activity detector to generate a total measure of functional activity in an integrated circuit and to determine whether or not the total measure of functional activity meets or exceeds a thermal limit of activity to generate an enable thermal throttling signal; and

a clock throttling controller coupled to the thermal activity detector and the free-running clock generator, the clock throttling controller to generate a throttled clock to couple to functional blocks of the integrated circuit for clocking circuitry therein, the clock throttling controller to gradually throttle the frequency of the throttled clock to circuitry of the functional blocks in response to the enable thermal throttling signal.

20. The clock generator of claim 19, wherein,

the clock throttling controller includes,

a linear feedback shift register connected in a loop to generate a clock gating control signal, the clock gating control signal to selectively mask out clock cycles in the throttled clock to gradually reduce its frequency and to selectively insert clock cycles into the throttled clock to gradually increase its frequency, and

a state machine coupled to the linear feedback shift register to control the selective masking out of clock cycles and the selective inserting of clock cycles in the throttled clock to gradually throttle the frequency down to shut OFF the throttled clock and gradually throttle the

frequency up from being shut OFF in response to the enable thermal throttling signal.

21. The clock generator of claim 20, wherein,

the clock throttling controller further includes,

a programmable counter to count a programmable delay time between changes in frequency of the throttled clock.